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A STUDY OF MICROELECTRONIC CIRCUIT PARAMETERS FOR NON-DIGITAL APPLICATIONS

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A STUDY OF

MICROELECTRONIC CIRCUIT PARAMETERS

FOR NON-DIGITAL APPLICATIONS

by

Timothy J. Cronin, Jr.
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Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

United States Naval Postgraduate School
Monterey, California

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This work is accepted as fulfilling
the thesis requirements for the degree of

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IN

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from the

United States Naval Postgraduate School

ABSTRACT

Microelectronics is introduced with definitions for some of the more controversial terms encountered in this new field.

Thin-film resistive elements are examined from the distributed parameter point of view and impedance functions for use in microcircuit analysis are derived.

A source of parasitic capacitance found in silicon integrated transistors is introduced by way of a sample calculation.

A small signal analysis for a simple linear amplifier stage is presented using microcircuit concepts along with transistor circuit theory.

Research for this paper was done, for the most part, at the Semiconductor Division, Hughes Aircraft Company, Newport Beach, California. For the opportunity to work in a microelectronics manufacturing environment, the author expresses sincerest thanks to Dr. D. A. Jenny, Mr. E. B. Gould III, and Mr. G. Wolfe of the Semiconductor Division. Special thanks is given to Mr. Dan Dooley and Mr. Ian Band for their valuable guidance.

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1. BACKGROUND AND DEFINITIONS

Encouraged by the development of semiconductor devices such as diodes and transistors, and spurred on by the need for smaller and lighter electronic packages for modern missile and space vehicle systems, the art of constructing electronic circuitry in less and less volume has made rapid advances in the past decade. The requirements for increased packing densities for electronic components (number of components per unit volume), along with rapidly evolving semiconductor techniques such as vacuum deposition, diffusion and epitaxial processes brought about the current state of circuit sophistication--Microelectronics.

Since there has been much confusion in the nomenclature associated with microelectronics, some definitions are given here. As yet, no standard set of terms has been set forth, so it is possible that a few of the definitions are biased toward the preferences of the author.

Microminiaturization may be thought of as that degree of miniaturization which will afford packing densities of more than 10^6 components per cubic foot of volume. Fig. 1 shows orders of magnitude for packing densities in several familiar areas and indicates the location of microminiature electronics in the scheme of things.

Microelectronics is a general term which refers to microminiaturization in electronics.

Integrated circuitry is that formed on or within a semiconductor material such as silicon. It includes active and passive elements formed

by diffusion, thin-film or epitaxial processes.

Thin-film elements are circuit elements which have been formed by depositing certain materials on passive supporting substrates.

Hybrid integrated circuitry, for this report, is that in which thin-film passive elements are combined with semiconductor integrated circuit active elements with an insulating oxide layer between. Fig. 2 shows a number of such hybrid circuits formed on a silicon wafer, with a Jefferson nickel included to indicate relative size.

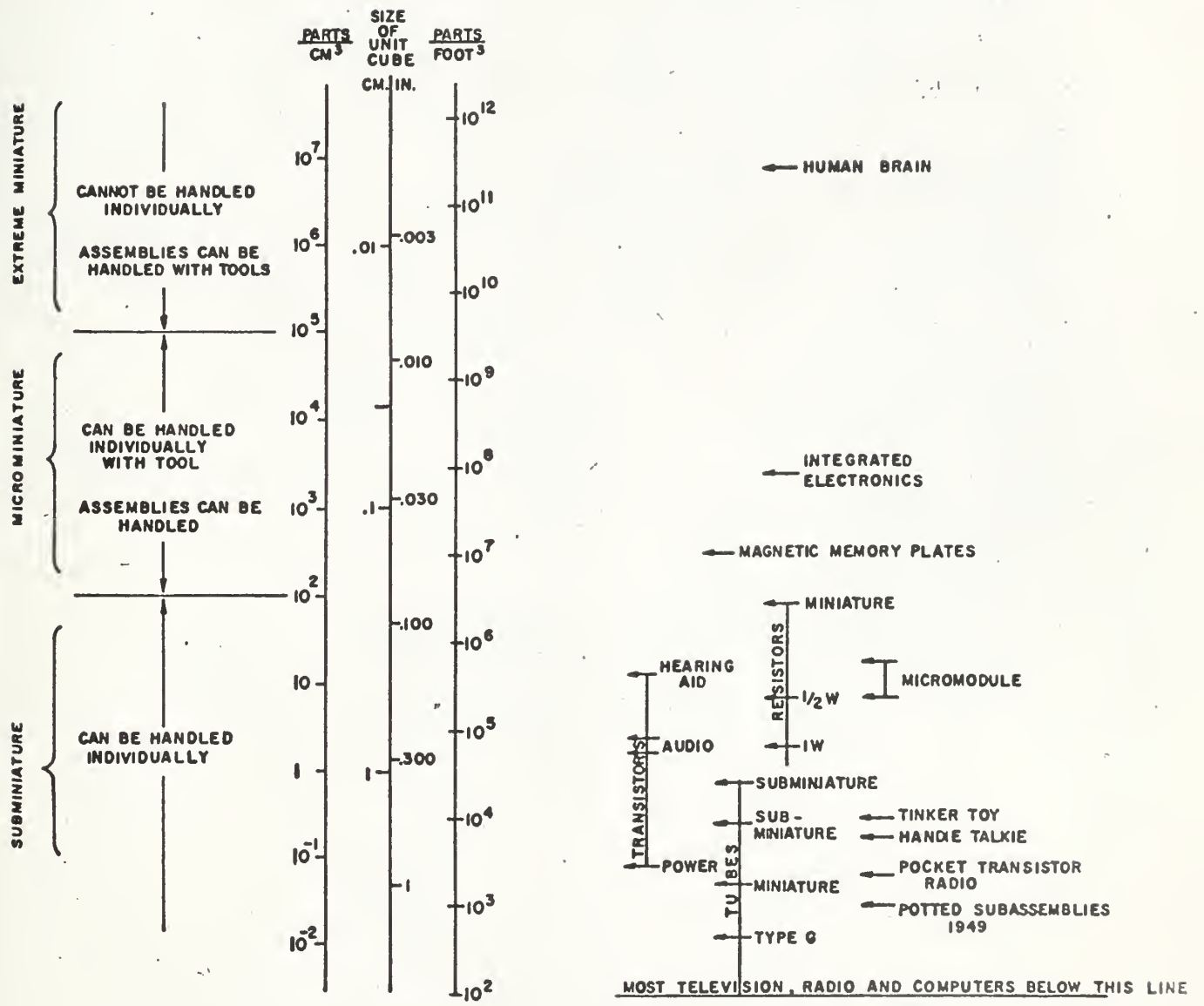


Fig. 1 Packing Densities of Electronic Components
(J. T. Wallmark, Proc. IRE, March 1960)

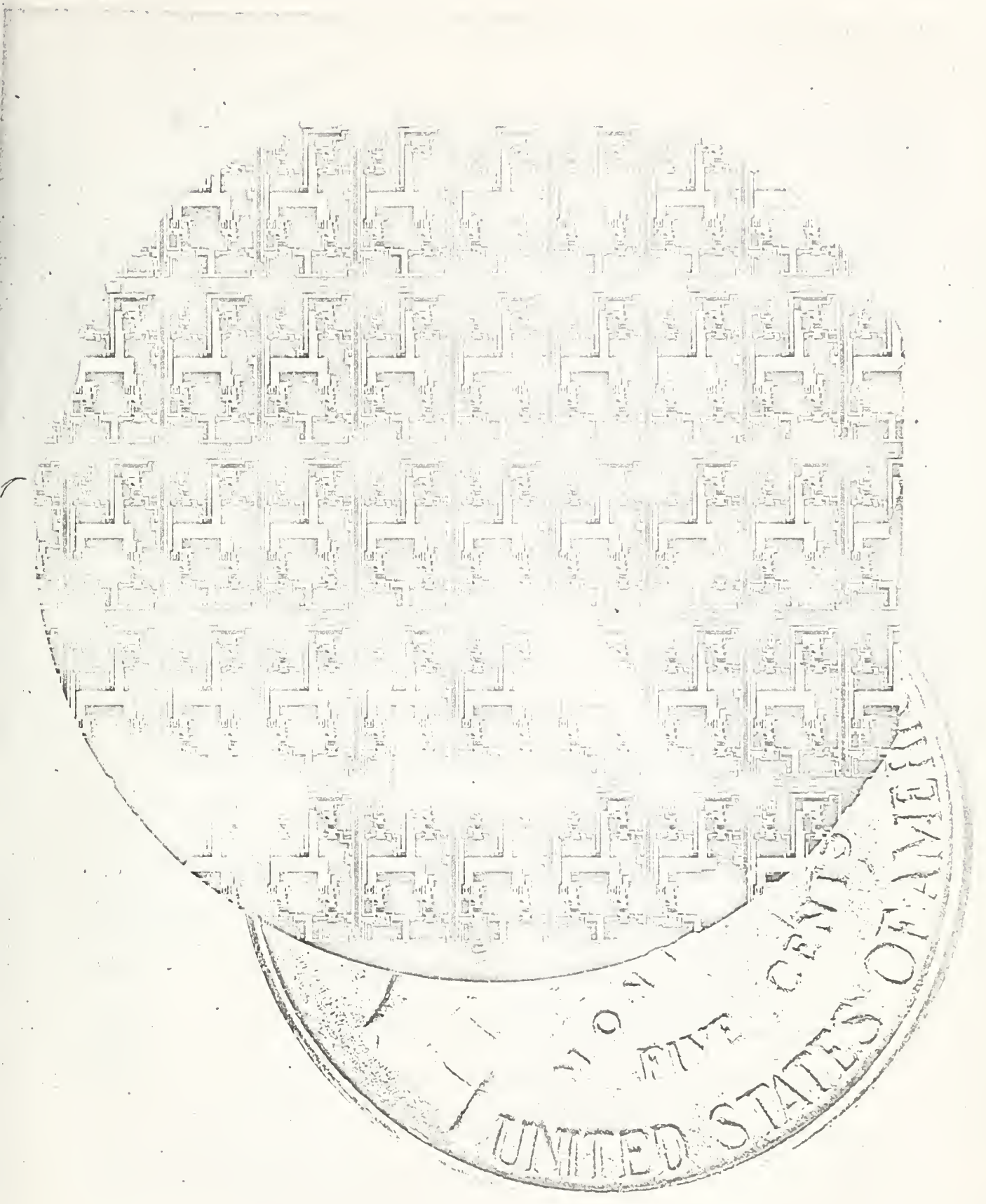


Fig. 2 Silicon Wafer Containing Hybrid Integrated Circuits.
(courtesy Semiconductor Division, Hughes Aircraft Company)

2. INTRODUCTION

As previously defined, microelectronics is a general term which refers to microminiaturization in electronics. Potential advantages to be gained by the use of microcircuitry instead of conventional electronic circuits include higher reliability, smaller size and weight, and lower costs /1/. One or more of these advantages is currently required for missile control and guidance systems, for aircraft radar and fire control systems, for high speed computers and for an almost endless array of other systems and sub-systems for military, commercial and aero-space ventures.

It is too early in the lifetime of microelectronics to make definite statements about the extent to which each of the major benefits claimed is actually realized in practice. For now, it is possible only to give a few reasons why these benefits are expected.

Higher reliability (the probability that a system will not fail during a specified period of time while operating under a given set of conditions /12/), probably the single most important feature claimed for microcircuitry, is expected because of the reduced number of connections and interconnection leads required as compared to conventional circuitry where poorly soldered or welded joints have long been a major factor in equipment failure rates. Overall system reliability improvement is anticipated because extensive use of circuit redundancy is made possible by virtue of the smaller weight and size of individual sub-assemblies. Tests, currently in progress, indicate that microcircuits are from 10 to 100 times more

reliable than similar circuits made up of conventional components /4/.

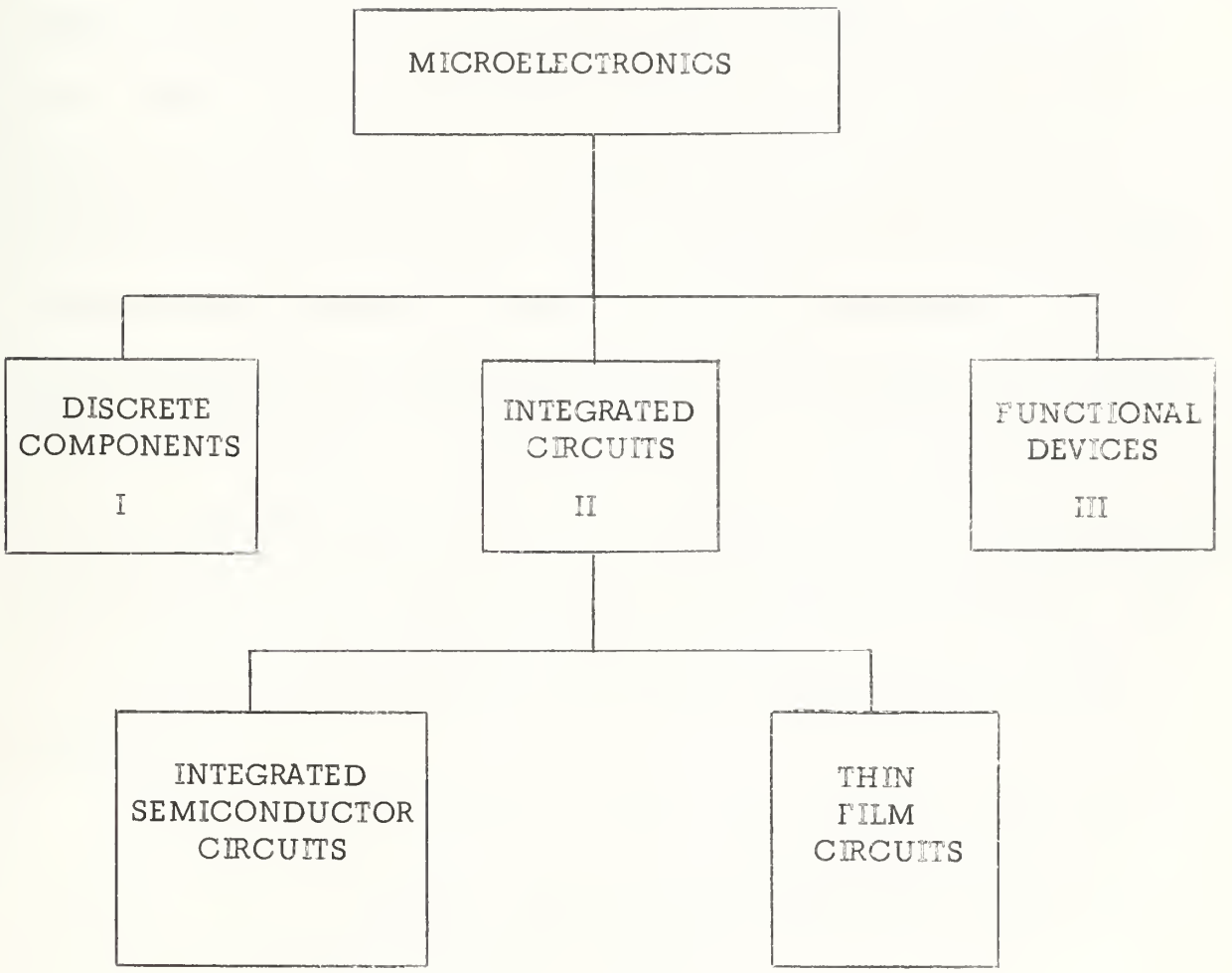
Smaller size and weight for microcircuits are obvious results from the increased packing densities.

The key to lower cost is a high volume of production. Initial tooling costs for microcircuit fabrication are high. Production of special circuits in limited quantities comes with a high price tag, but if industrial and military computers are built with microminiature circuits, the demand for large volumes of similar circuits will make the production costs drop. Standardization of a number of non-digital circuits will make possible lower costs in that area.

Microelectronics may be categorized by three major approaches: the miniature discrete component approach, the integrated circuit approach and a functional device approach. A fourth, through not entirely separate approach, combines some of the features of the others into a hybrid approach /9/. These classifications are depicted graphically in Fig. 3.

Each of the approaches mentioned has been found to have merit for particular applications, so it is difficult to label any one as superior. Since professional literature of recent months abounds in papers and articles concerning the approaches to microminiaturization, a complete discussion of the subject is omitted here.

In the integrated circuit approach, the most widely used structure at the present time is the hybrid integrated circuit. An outline of the steps required to produce this type of circuit is given in Appendix B.



Hybrid approach: combination of I and II or
combinations within II

Fig. 3 Classifications of Microelectronics

Technological advances have traditionally brought with them problems, old and new, inherent and environmental. This is true also for microelectronics. Early theories held that interactions among circuit elements under operating conditions would remain the same if all components were reduced proportionately in size, and that a given input would give the same output, no matter what the size of the circuit elements. Unfortunately, these ideas were found inadequate when applied to thin-film and semiconductor integrated circuits. Individual elements of semiconductor integrated circuits are isolated from one another by junction diode action. Interconnection schemes introduce intercoupling capacitances. Resistors and capacitors are not lumped elements but must be treated as distributed parameter components. Inductors have defied current thin-film and integrated circuit processes due to the extremely reduced volumes involved. Analytical models for microcircuitry have not yet become available. The list of problems appears endless; the future holds promise for timely solutions.

In order to show how ordinary circuit concepts may be molded to provide a means of analyzing microelectronic non-digital circuits, the author has addressed himself to the tasks of:

a) showing the impedance functions for the distributed parameter passive networks which describe thin-film resistive elements,

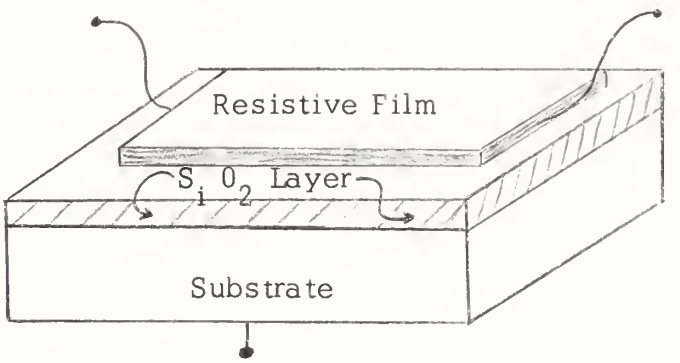
b) indicating the type calculation needed to describe the capacitive effects introduced in silicon integrated circuits by the junction

diode isolation regions, and

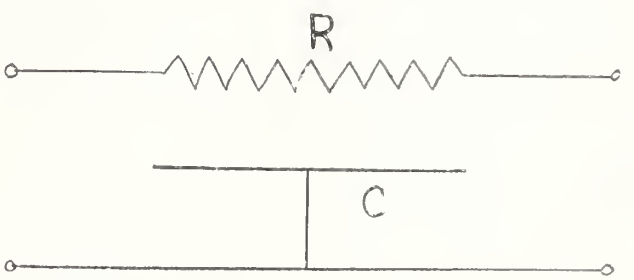
c) performing a small signal analysis of a simple microcircuit linear amplifier stage, considering microelectronic concepts and transistor circuit theory.

3. DERIVATION OF IMPEDANCE FUNCTIONS FOR THIN-FILM RESISTIVE ELEMENTS USED IN HYBRID INTEGRATED CIRCUITRY /2,7,10,17/

Thin-film resitors are produced by depositing a resistive material such as nichrome on some supporting structure. For hybrid integrated circuitry, the supporting structure is a block or wafer of silicon which contains the circuit active elements. A layer of silicon dioxide is used for separating the active from the thin-film passive components. A typical structure is shown in the sketch of Figure 4 (a).



(a) Thin-Film Structure



(b) Schematic Symbol for (a)

Fig. 4 Thin Film Resistor

The silicon dioxide (SiO_2) layer acts as a dielectric between the resistive material on the top and the supporting substrate. This gives rise to a capacitance. The resistive-capacitive nature of the element is shown in the schematic symbol of Figure 4 (b).

The resistance and capacitance of the thin-film element are distributed throughout its length with the total resistance being R and the total capacitance being C. In the structure, phenomena occur on a differential basis so the element will have a response similar to that of a leakage-free non-inductive transmission line. Assuming a transmission line of length d, the resistance and capacitance per unit length is then give by

$$r = R/d \qquad \text{and} \qquad c = C/d$$

Consider that a section of transmission line to represent the thin-film element has the parameters shown in Figure 5.

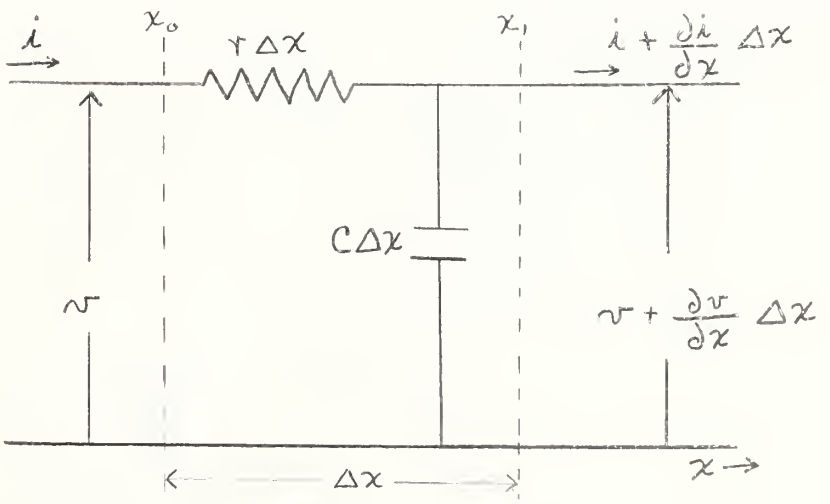


Fig. 5 Transmission line section representing a thin-film resistor

It is desired that an impedance matrix be derived from the parameters of Fig. 5 which will be useful for representing the distributed parameter elements of thin-film microcircuitry. Since non-digital applications are of primary interest in this paper, a set of functions which will reflect variations with frequency are desired.

The change in current from x_o to $x_1 = x_o + \Delta x$ is

$$\frac{\partial i}{\partial x} \Delta x = - c \Delta x \frac{\partial v}{\partial t} \tag{1}$$

and the voltage drop from x_o to $x_o + \Delta x$ is

$$\frac{\partial v}{\partial x} \Delta x = - r i \Delta x \tag{2}$$

where $v = v(t, x)$ and $i = i(t, x)$.

Dividing Equations (1) and (2) by Δx gives

$$\frac{\partial i}{\partial x} = - c \frac{\partial v}{\partial t} \tag{3}$$

and

$$\frac{\partial v}{\partial x} = - r i \tag{4}$$

The Laplace Transforms of Equations (3) and (4) are

$$\frac{\partial I(s)}{\partial x} = - sc\, V(s) \tag{5}$$

and

$$\frac{\partial V(s)}{\partial x} = - r\, I(s) \tag{6}$$

where initial conditions are assumed to be

$$I(0) = V(0) = 0$$

Now, since v and i are both functions of the real variable x, Equations (5) and (6) may be differentiated with respect to x, giving:

$$\frac{\partial^2 V(s,x)}{\partial x^2} = -r\, \frac{\partial I(s,x)}{\partial x} = sc\, r\, V(s,x) \tag{7}$$

Letting $scr = \gamma^2$, then

$$\frac{\partial^2 V(s,x)}{\partial x^2} = \gamma^2 V(s,x) \tag{8}$$

and

$$\frac{\partial^2 I(s,x)}{\partial x^2} = \gamma^2 I(s,x) \tag{9}$$

The general solution for the differential Equation (8) is

$$V(s,x) = \left(A e^{\gamma x} + B e^{-\gamma x}\right) \tag{10}$$

From Equation (6),

$$I(s,x) = -1/r \quad \frac{\partial V(s,x)}{\partial x}$$

thus $$I(s,x) = -\frac{\gamma}{r}\left(A e^{\gamma x} - B e^{-\gamma x}\right) \tag{11}$$

Letting $\frac{\gamma}{r} = \frac{1}{Z_0}$, and since x = 0 at the input and of the line,

$$V(s,0) = A + B \tag{12}$$

$$I(s,0) = -\frac{1}{Z_0}\left(A - B\right) \tag{13}$$

whence,

$$A = \frac{1}{2}\left[V(s,0) - Z_0 I(s,0)\right] \tag{14}$$

$$B = \frac{1}{2}\left[V(s,0) + Z_0 I(s,0)\right] \tag{15}$$

Substituting (14) and (15) into (10) and (11), the voltage and current at any point in the line may be determined as a function of the input voltage and current.

$$V(s,x) = \frac{1}{2} e^{\gamma x}\left[V(s,0) - Z_0 I(s,0)\right]$$

$$+ \frac{1}{2} e^{-\gamma x}\left[V(s,0) + Z_0 I(s,0)\right]$$

$$= V(s,0)\left[\frac{e^{\gamma x} + e^{-\gamma x}}{2}\right] - Z_0 I(s,0)\left[\frac{e^{\gamma x} - e^{-\gamma x}}{2}\right]$$

or

$$V(s,x) = V(s,0)\cosh \gamma x - Z_0 I(s,0)\sinh \gamma x \qquad (16)$$

and, similarly,

$$I(s,x) = -\frac{1}{Z_0} V(s,0)\sinh \gamma x + I(s,0)\cosh \gamma x \qquad (17)$$

For thin-film resistors to be used in circuits such as the amplifier stage to be discussed in a later section, there are two basic connections of the network of Fig. 4 which are useful. These are shown in Fig. 6.

Configuration (a) is that which may be employed when the element is used for coupling and (b) is that which may be used for the case where one end of the resistor is tied to some fixed potential or ground.

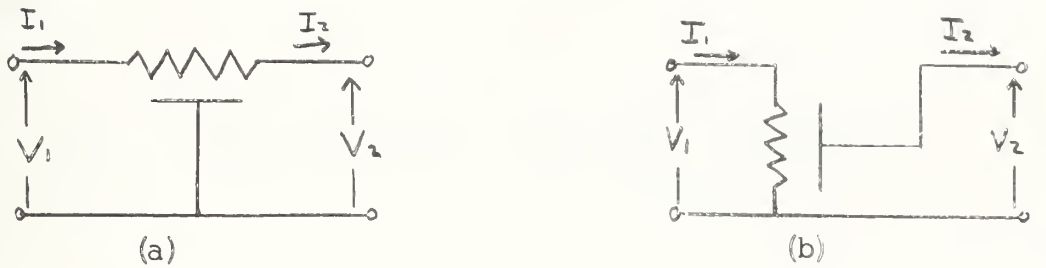


Fig. 6. Thin-Film resistor connections

In Fig. 6,

$$V_1 = V(s,0) \qquad V_2 = V(s,d)$$

$$I_1 = I(s,0) \qquad I_2 = I(s,d)$$

d is the end of the distributed element

$$\theta = \gamma d = \sqrt{rcs}\, d = \sqrt{sRC}$$

Equations (16) and (17) may now be written as:

$$V_2 = V_1 \cosh \theta - Z_0 I \sinh \theta \tag{18}$$

$$I_2 = -\frac{V_1}{Z_0}\sinh\theta + I_1\cosh\theta \qquad (19)$$

For configuration (a) of Fig. 6, manipulation of Equations (18) and (19) gives

$$V_1 = Z_0 I_1 \coth\theta - Z_0 I_2 \operatorname{cosech}\theta \qquad (20)$$

$$V_2 = Z_0 I_1 \operatorname{cosech}\theta - Z_0 I_2 \coth\theta \qquad (21)$$

or in matrix form,

$$Z_0 \begin{bmatrix} \coth\theta & -\operatorname{cosech}\theta \\ \operatorname{cosech}\theta & -\coth\theta \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (22)$$

For configuration (b) of Fig. 6, rearranging the terminals gives the following parameters:

$$I_1' = I_1 \qquad V_1' = V_1 - V_2$$

$$I_2' = I_1 - I_2 \qquad V_2' = -V_2$$

The rearrangement which gives these parameters is shown in Fig. 7.

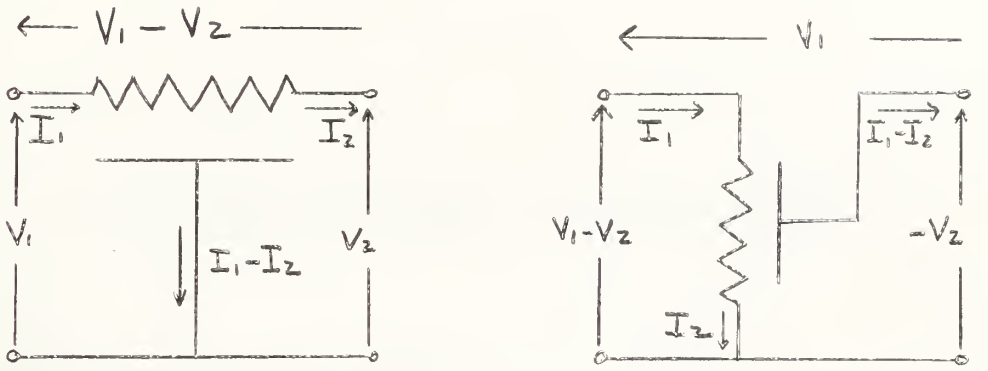


Fig. 7. Rearrangement of terminals

These new parameters when applied to Equations (20) and (21) result in the following matrix form:

$$Z_o \begin{bmatrix} 2\tanh\frac{\theta}{2} & -\tanh\frac{\theta}{2} \\ \tanh\frac{\theta}{2} & -\coth\theta \end{bmatrix} \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} \tag{23}$$

From these solutions, those equations needed for specific analytical applications may be taken directly or may be derived as necessary. For example:

Considering configuration 6 (b),

From (23),

$$V_1' = Z_0 \left(2 \tanh \frac{\theta}{2} I_1' - \tanh \frac{\theta}{2} I_2' \right) \qquad (24)$$

$$V_2' = Z_0 \left(\tanh \frac{\theta}{2} I_1' - \coth \theta I_2' \right) \qquad (25)$$

Case I. . . . Substrate grounded, i.e., $V_2' = 0$

$$\frac{I_2'}{I_1'} = \frac{\tanh \frac{\theta}{2}}{\coth \theta}$$

Letting $Z_0 = R/\theta$ and $Z_I = V_1'/I_1'$

$$Z_I = Z_0 \left[2 \tanh \frac{\theta}{2} - \frac{\tanh^2 \frac{\theta}{2}}{\coth \theta} \right]$$

$$= Z_0 \left[\left(1 + \tanh^2 \frac{\theta}{2} \right) \tanh \theta - \frac{\tanh^2 \frac{\theta}{2}}{\coth \theta} \right]^*$$

$$= Z_0 \left[\tanh \theta + \tanh^2 \frac{\theta}{2} \tanh \theta - \tanh^2 \frac{\theta}{2} \tanh \theta \right]$$

$$= Z_0 \tanh \theta$$

*Note: $2 \tanh \frac{\theta}{2} = \left(1 + \tanh^2 \frac{\theta}{2} \right) \tanh \theta$ /20/.

Whence,

$$Z_I = \frac{R}{\theta} \tanh \theta \tag{26}$$

Case II...Isolated Substrate, i.e., $I_2' = 0$

From (23) and (24)

$$V_1' = 2 Z_o I_1' \tanh \frac{\theta}{2}$$

If $Z_{II} = \frac{V_1'}{I_1'}$ then,

$$Z_{II} = 2 Z_o \tanh \frac{\theta}{2}$$

or

$$Z_{II} = \frac{2R}{\theta} \tanh \frac{\theta}{2} \tag{27}$$

4. CALCULATION OF COLLECTOR TO SUBSTRATE CAPACITANCE FOR A DOUBLE DIFFUSED SILICON INTEGRATED TRANSISTOR /11,13,17,19,22/

Figure 8 shows a side view of an isolated, integrated transistor which has been constructed by a double diffusion process.

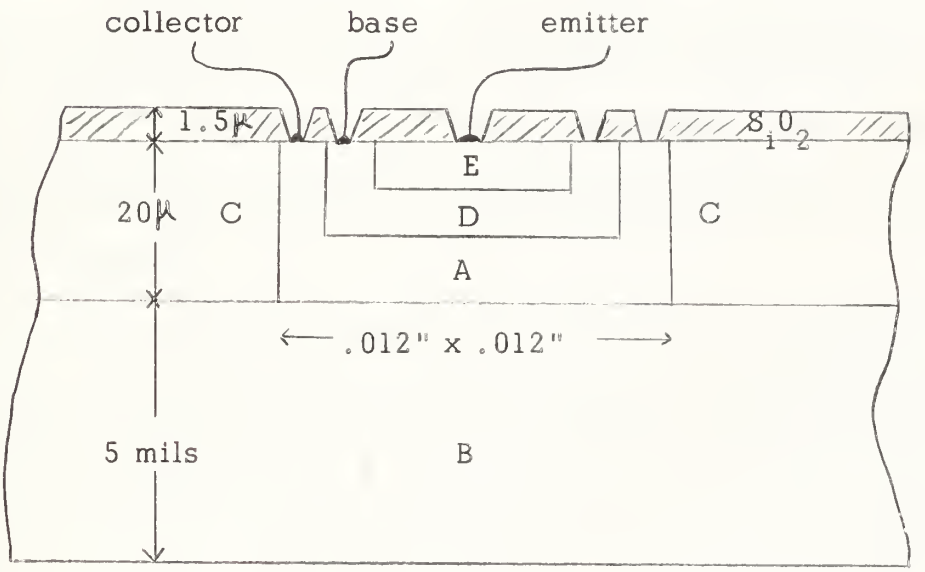


Fig. 8 Double diffused integrated transistor

In forming the transistor, a layer of n-doped silicon (region A) is epitaxially grown on top of a p-doped silicon substrate (region B). Isolation from other diffused elements of the same wafer is provided by a region called a fence (region C) which is formed by diffusion boron or some other p-dopant into the epitaxial layer around the element to be isolated. Another boron diffusion is required to form the p-doped transistor base (region D). The emitter of the transistor is formed by a phosphorus (n-dopant) diffusion (region E). A silicon dioxide (SiO_2) layer is deposited over the entire upper surface of the wafer to provide isolation between the active integrated

elements and any passive networks or interconnection leads which may be required to complete a circuit. Holes may be etched in the oxide at points where connections to the active element must be made /17/.

The integrated structure of Fig. 8 is highly idealized. Junctions made by diffusion processes are, unfortunately, not abrupt as shown. These junctions are best described by gaussian and/or complementary error function distributions /21/. Since the gaussian approximation lends itself to ease of manipulation, it is assumed for the following discussion that this distribution is adequate.

To calculate the capacitance associated with the diffusion junctions, the interface areas between region A and regions B and C are of interest. The calculation will result in a collector-to-substrate capacitance value. Some representative dimensions are shown on the drawing of Fig. 8. Representative values of impurity concentrations (doping) at the surfaces of each region are given in Table I /17/.

Table I

Impurity Concentrations

Region	N_p (p-dopant) atoms/m^3	N_n (n-dopant) atoms/m^3
A	–	3×10^{16}
B	4×10^{15}	–
C	8×10^{18}	–
D	4×10^{18}	–
E	–	3×10^{20}

The interface areas of the junctions between region A and regions B and C for the transistor structure are as follow:

A-B junction.....$12x12x25.4^2x10^{-8}cm^2 = 9.29x10^{-4}cm^2$

A-C junction.....$12x20x4x25.4x10^{-8}cm^2 = 2.44x10^{-4}cm^2$

For the capacitance calculations, the following definitions and equations apply:

N_1.....doping concentration before diffusion

N_0.....doping concentration after diffusion

x_j.....depth to junction

D.....a diffusion constant for the diffusing impurity

t.....time (sec)

L.....$2\sqrt{Dt}$ the impurity diffusion length

y_j.....x_j/L

ϵ.....dielectric constant, for silicon $0.98x10^{-12}$ f/cm

q/ϵ.....for silicon, $1.62x10^{-7}$ v. cm.

v.....applied voltage

For junction A-B, $x_j \simeq 8\,\mu$, $N_1 \simeq 4x10^{14}$, $N_0 \simeq 3x10^{16}$

For junction A-C, $x_j \simeq 12\,\mu$*, $N_1 \simeq 3x10^{16}$, $No \simeq 3x10^{20}$

Assuming a gaussian distribution for the impurities near the junctions,

$$e^{-y_j^2} = \frac{N_1}{N_0} \qquad (28)$$

*The horizontal location of the diffused junction is taken here to be approximately 0.6 times the depth of the fence region /17/.

which for the junctions above give:

For junction A-B $e^{-y_j^2} = \frac{4 \times 10^{14}}{3 \times 10^{16}} = 1.33 \times 10^{-2}$

$$y_j^2 = 4.32$$

For junction A-C $e^{-y_j^2} = \frac{3 \times 10^{16}}{3 \times 10^{20}} = 10^{-4}$

$$y_j^2 = 7.28$$

As might be expected, the capacitances of the diode junctions are dependent upon the reverse bias voltages applied. Curves giving the relationships between space charge fields and applied voltages have been developed /21/. In order to use the curves, some normalized capacitance and voltage values are required, defined as:

$$C_N = 2\epsilon \frac{y_j^2}{x_j} \quad \text{and} \quad V_N = \frac{q}{\epsilon} \frac{N_1}{4} \frac{x_j^2}{y_j^4} \tag{29}$$

For junction A-B:

$$C_N = \frac{0.98 \times 10^{-12} \times 2 \times 4.32}{8 \times 10^{-4}} = 10.2 \times 10^{-9}$$

$$V_N = \frac{1.62 \times 10^{-7} \times 4 \times 10^{14} \times 64 \times 10^{-8}}{4 \times (4.32)^2} = 0.554$$

For junction A-C:

$$C_N = \frac{0.98 \times 10^{-12} \times 2 \times 7.82}{12 \times 10^{-4}} = 12.7 \times 10^{-9}$$

$$V_N = \frac{1.62 \times 10^{-7} \times 3 \times 10^{16} \times 144 \times 10^{-8}}{4 \times (7.82)^2} = 28.7$$

The curves of Reference 21 give values of a dummy variable $(u_1 - u_2)$ for V/V_N where V is the total voltage across the junction. Capacitance is then defined as

$$C = \frac{A\, C_N}{(u_1 - u_2)} \quad \text{pf.} \tag{30}$$

Using the information above and the curve for $(u_1 - u_2)$ vs V/V_N, capacitance values for various applied voltages were determined and are listed in tables II and III.

The total collector-to-substrate capacitance is the sum of the two capacitance values calculated for each voltage. A curve of capacitance vs bias voltage is shown on the graph of Fig. 9.

From the curves of Fig. 9, it can be seen that the amount of inherent capacitance associated with the junction diode interfaces of an integrated transistor can be minimized by suitable choice of biasing conditions of the microcircuit.

Table II

Calculated capacitance values for junction A-B

Applied Voltage (volts)	V*	V/V_N	(u_1-u_2)	$C=\frac{A\ C_N}{(u_1-u_2)}$
0	0.7	1.26	2.5	3.78 pf
1	1.7	3.07	3.6	2.63
3	3.7	6.68	4.7	2.01
6	6.7	11.00	5.8	1.63
12	12.7	22.90	7.7	1.23
15	15.7	28.40	8.5	1.11
20	20.7	37.40	9.6	0.985

Table III

Calculated capacitance values for junction A-C

Applied Voltage (volts)	V*	V/V_N	(u_1-u_2)	$C=\frac{A\ C_N}{(u_1-u_2)}$
0	0.7	0.024	0.66	4.7 pf
1	1.7	0.059	0.89	3.47
3	3.7	0.129	1.15	2.69
6	6.7	0.212	1.38	2.24
12	12.7	0.443	1.75	1.77
15	15.7	0.546	1.90	1.63
20	20.7	0.722	2.05	1.51

*The total voltage includes 0.7 volts for silicon junction

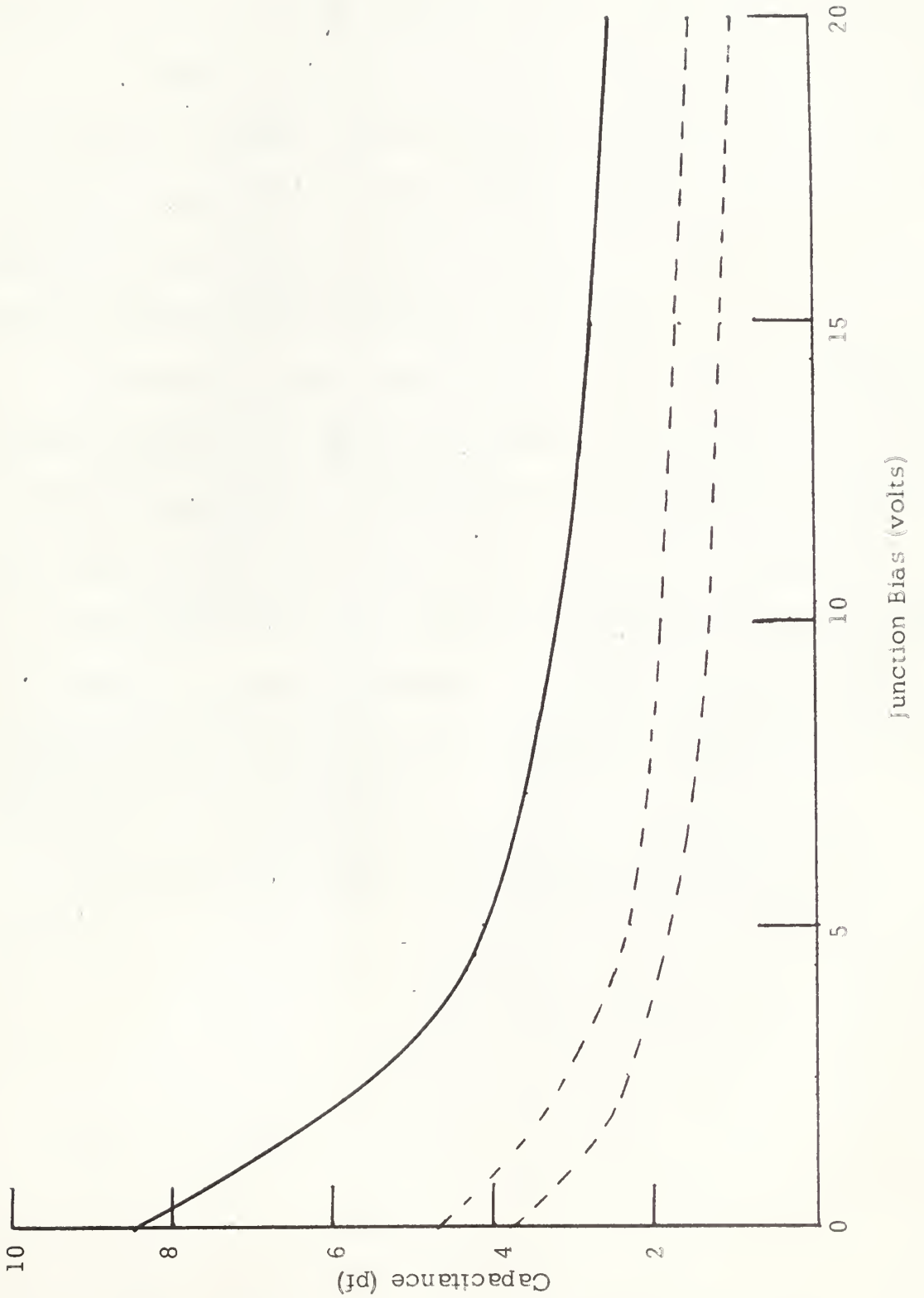


Fig. 9 Graph of Collector to Substrate Capacitance vs Junction Bias Voltage

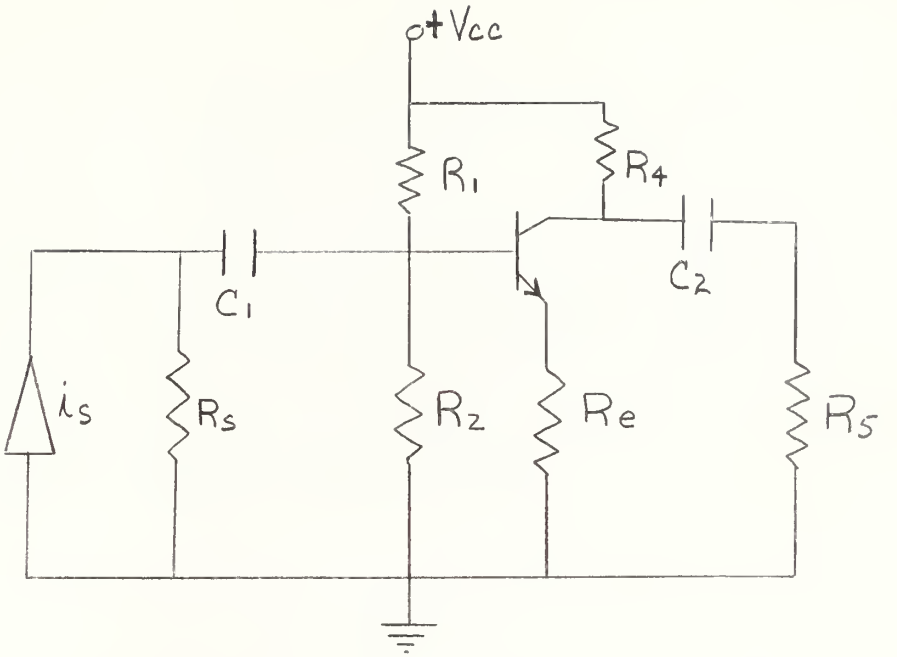
5. SMALL SIGNAL ANALYSIS OF A MICROCIRCUIT AMPLIFIER STAGE /5,6,8,18/

This section is intended to show the type of considerations required for analyzing microminiature integrated circuits. Basically, the problem is that the lumped R and C of ordinary circuit theory must be replaced by distributed R-C sections, the impedances of which include non-rational hyperbolic functions of a complex frequency variable. This immediately indicates that any analysis must be kept simple in order to prevent resultant expressions from becoming too cumbersome.

A simple single-stage, common emitter amplifier circuit was selected for examination. This simple circuit enables one to become aware of the complexity of microcircuit analysis while still allowing for a mathematical treatment without resorting to long involved computer programming.

To facilitate a reasonable analytical investigation, the basic circuit is reduced by a number of approximations and simplifying assumptions, so that a complete rigid mathematical treatment is rejected in favor of a more useful approximate solution.

The transistor R-C coupled amplifier stage of Fig. 10 was first considered.



R_s is the output resistance of the preceeding stage and R_5 is an a-c load resistance

Fig. 10 R-C Coupled amplifier stage

Since present day microcircuit capacitors require large areas to achieve appreciable capacitance, it was desirable to eliminate, if possible, the D-C blocking capacitors C_1 and C_2. Then, employing direct coupling, the need for the biasing resistors R_1 and R_2 was eliminated. For the single stage, these omissions would probably cause stability problems, but it is assumed that most applications will require cascaded stages, and feedback networks or also neutralization networks would be incorporated to assist in the reduction of the stability problems. Here one is interested in showing how complex even the simplest of

circuits may become when microcircuit concepts are considered, so the stabilization problem was not treated.

The thin-film resistors which would be used to construct a microcircuit amplifier cannot be treated as lumped elements because of their distributed nature. Instead, the impedance functions derived in Section 2 are used to replace the resistors of the amplifier circuits.

An amplifier stage such as that shown schematically in Fig. 11 results from the foregoing consideration.

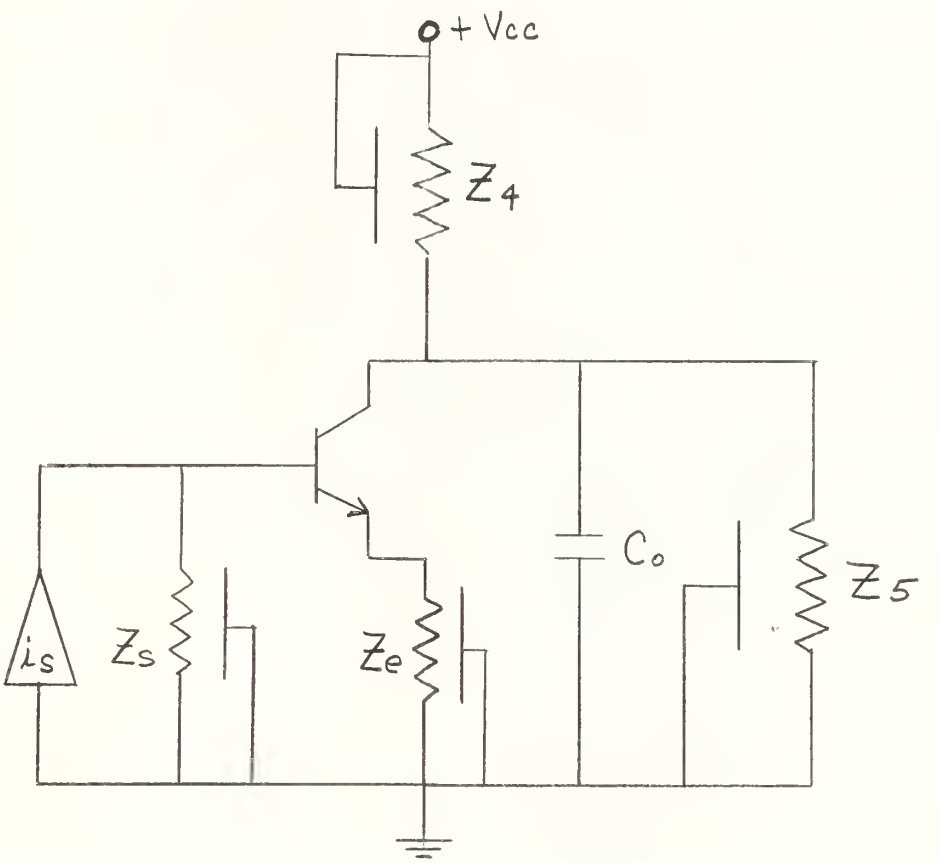


Fig. 11 Amplifier stage with distributed elements

In order to analyze the circuit, the transistor was replaced by a hybrid-pi equivalent circuit model. This particular model was chosen since it appears to be one of the most convenient equivalent circuit models for small signal, common-emitter circuit use /8/. The resultant equivalent circuit for the microcircuit amplifier stage is shown in Fig. 12. It has been assumed for this circuit that a suitable bias voltage was applied to keep the collector-to-substrate capacitance to a small enough value to be neglected.

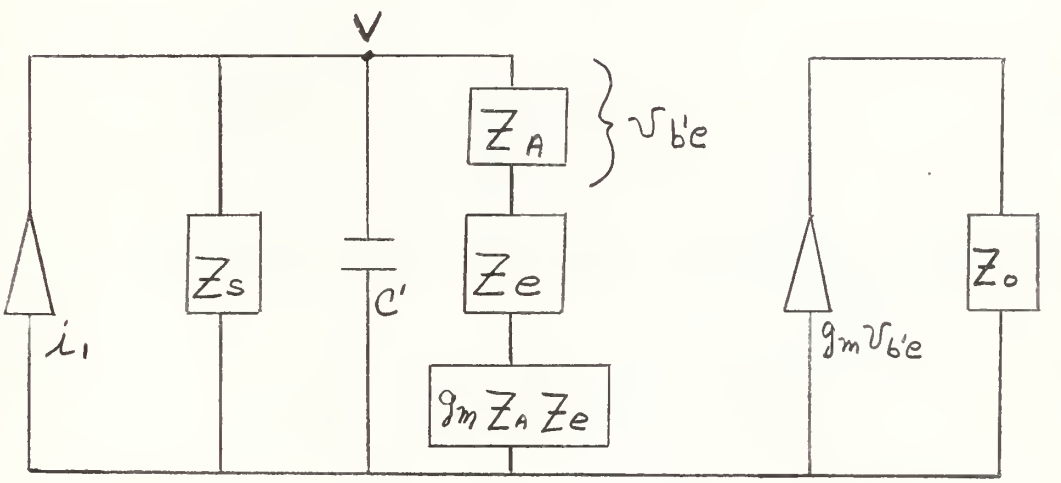


Fig. 12 Equivalent circuit for amplifier stage

In Fig. 12, Z_o is the parallel combination of Z_4, Z_5, and X_{co} of Fig. 11.

$$C' = C_{b'c} \left(1 + \frac{g_m Z_o Z_A}{Z_b}\right) \qquad (31)$$

$$Z_A = \frac{r_{b'e}\ \omega_{\beta o}}{j\omega + \omega_{\beta o}} \tag{32}$$

$$Z_b \triangleq Z_A + Z_e(1 + g_m Z_A) \tag{33}$$

$$\omega_{\beta o} = \frac{1}{r_{b'e}\ C_{b'c}} \tag{34}$$

If the operating frequency is limited to allow the assumption that

$$1/\omega C' >> Z_b >> Z_s \tag{35}$$

then,

$$V = i_1 Z_s \tag{36}$$

and

$$V_{b'e} = V(Z_A/Z_b) = \frac{i_1 Z_A Z_s}{Z_b} \tag{37}$$

Now,

$$i_2 = g_m V_{b'e} \tag{38}$$

and from (37),

$$i_1 = \frac{V_{b'e} Z_b}{Z_A Z_S} \tag{39}$$

Thus,

$$i_2 / i_1 = \frac{g_m Z_A Z_S}{Z_b} \tag{40}$$

In ordinary transistor circuit work, it is often reasonable to assume that $Z_b \simeq g_m Z_A Z_e$

Applying this idea here gives a simple current gain expression

$$\frac{i_2}{i_1} = \frac{Z_S}{Z_e} \tag{41}$$

In Section 3, it is shown that the impedance expressions for the thin-film resistor networks were:

$$Z = \frac{R}{\theta} \tanh \theta \qquad \text{for grounded substrate} \tag{42}$$

$$Z = \frac{2R}{\theta} \tanh \frac{\theta}{2} \qquad \text{for isolated substrate} \tag{43}$$

Using this information, Equation (41) becomes

$$\frac{i_2}{i_1} = \frac{R_s/\theta_s \tanh \theta_s}{R_e/\theta_e \tanh \theta_e} \quad \text{for grounded substrate} \tag{44}$$

and

$$\frac{i_2}{i_1} = \frac{R_s/\theta_s \tanh \theta_s/2}{R_e/\theta_e \tanh \theta_e/2} \quad \text{for isolated substrate} \tag{45}$$

Since $\theta = (j\omega RC)^{1/2}$, the gain expression contains non-rational hyperbolic functions of the complex variable $j\omega$. In Appendix A, it is shown that the complex expression for the distributed parameter impedances may be written as an absolute magnitude with an associated phase angle. For the current gain, the ratio of two complex impedances give a similar type of expression.

For the grounded substrate case, the magnitude of the current gain is,

$$\left|\frac{i_2}{i_1}\right| = \frac{\dfrac{R_s}{(\omega R_s C_s)^{1/2}} \left[\dfrac{\cosh\sqrt{2\omega R_s C_s} - \cos\sqrt{2\omega R_s C_s}}{\cosh\sqrt{2\omega R_s C_s} + \cos\sqrt{2\omega R_s C_s}}\right]^{1/2}}{\dfrac{R_e}{(\omega R_e C_e)^{1/2}} \left[\dfrac{\cosh\sqrt{2\omega R_e C_e} - \cos\sqrt{2\omega R_e C_e}}{\cosh\sqrt{2\omega R_e C_e} + \cos\sqrt{2\omega R_e C_e}}\right]^{1/2}} \tag{46}$$

with a phase angle given by

$$\angle\left(\frac{i_2}{i_1}\right) = \tan^{-1}\left[\frac{\sin\sqrt{2\omega R_s C_s} - \sinh\sqrt{2\omega R_s C_s}}{\sin\sqrt{2\omega R_s C_s} + \sinh\sqrt{2\omega R_s C_s}}\right]$$

$$-\tan^{-1}\left[\frac{\sin\sqrt{2\omega R_e C_e} - \sinh\sqrt{2\omega R_e C_e}}{\sin\sqrt{2\omega R_e C_e} + \sinh\sqrt{2\omega R_e C_e}}\right] \quad (47)$$

For the isolated substrate case, the magnitude of the current gain is

$$\left|\frac{i_2}{i_1}\right| = \frac{\dfrac{R_s}{(\omega R_s C_s)^{1/2}}\left[\dfrac{\cosh\sqrt{\frac{\omega R_s C_s}{2}} - \cos\sqrt{\frac{\omega R_s C_s}{2}}}{\cosh\sqrt{\frac{\omega R_s C_s}{2}} + \cos\sqrt{\frac{\omega R_s C_s}{2}}}\right]^{1/2}}{\dfrac{R_e}{(\omega R_s C_s)^{1/2}}\left[\dfrac{\cosh\sqrt{\frac{\omega R_e C_e}{2}} - \cos\sqrt{\frac{\omega R_e C_e}{2}}}{\cosh\sqrt{\frac{\omega R_e C_e}{2}} + \cos\sqrt{\frac{\omega R_e C_e}{2}}}\right]^{1/2}} \quad (48)$$

with a phase angle given by

$$\angle\left(\frac{i_2}{i_1}\right) = \tan^{-1}\left[\frac{\sin\sqrt{\frac{\omega R_s C_s}{2}} - \sinh\sqrt{\frac{\omega R_s C_s}{2}}}{\sin\sqrt{\frac{\omega R_s C_s}{2}} + \sinh\sqrt{\frac{\omega R_s C_s}{2}}}\right]$$

$$-\tan^{-1}\left[\frac{\sin\sqrt{\frac{\omega R_e C_e}{2}} - \sinh\sqrt{\frac{\omega R_e C_e}{2}}}{\sin\sqrt{\frac{\omega R_e C_e}{2}} + \sinh\sqrt{\frac{\omega R_e C_e}{2}}}\right] \quad (49)$$

Equations (46) through (49) contain several variables (Re, Ce, Rs, Cs, and ω). In order to display changes in gain with frequency, the R and C values should be known. For specific circuits, these will be known quantities, but here, in order to retain some generality, ratios of Rs to Re are used and curves will be plotted for gain vs frequency where a frequency variable ω Re Ce is used.

Selection of a ratio of resistance will also dictate a ratio of capacitance since the capacitance for a thin-film element is a function of the area covered by the element. This relationship is indicated on the graph of Fig. 13 /17/.

Figure 14 and Fig. 16 show the variation of current gain for three selected values of Rs/Re as frequency is varied. For convenience, the gain curves are given in db below midband or dc gain. Frequency variation is lumped with Re and Ce so that the frequency parameter is ω Re Ce. The curves were obtained by direct substituion of values in Equations (46) and (48) /6/.

Equations (47) and (48) were used to obtain phase angle curves for frequency variation. These curves are plotted on graphs of Fig. 15 and Fig. 17.

For Figs. 14 through 17, the curve traces are numbered as follows:

I.....for Rs = 3 Re
II.....for Rs = 5 Re
III .....for Rs = 8 Re

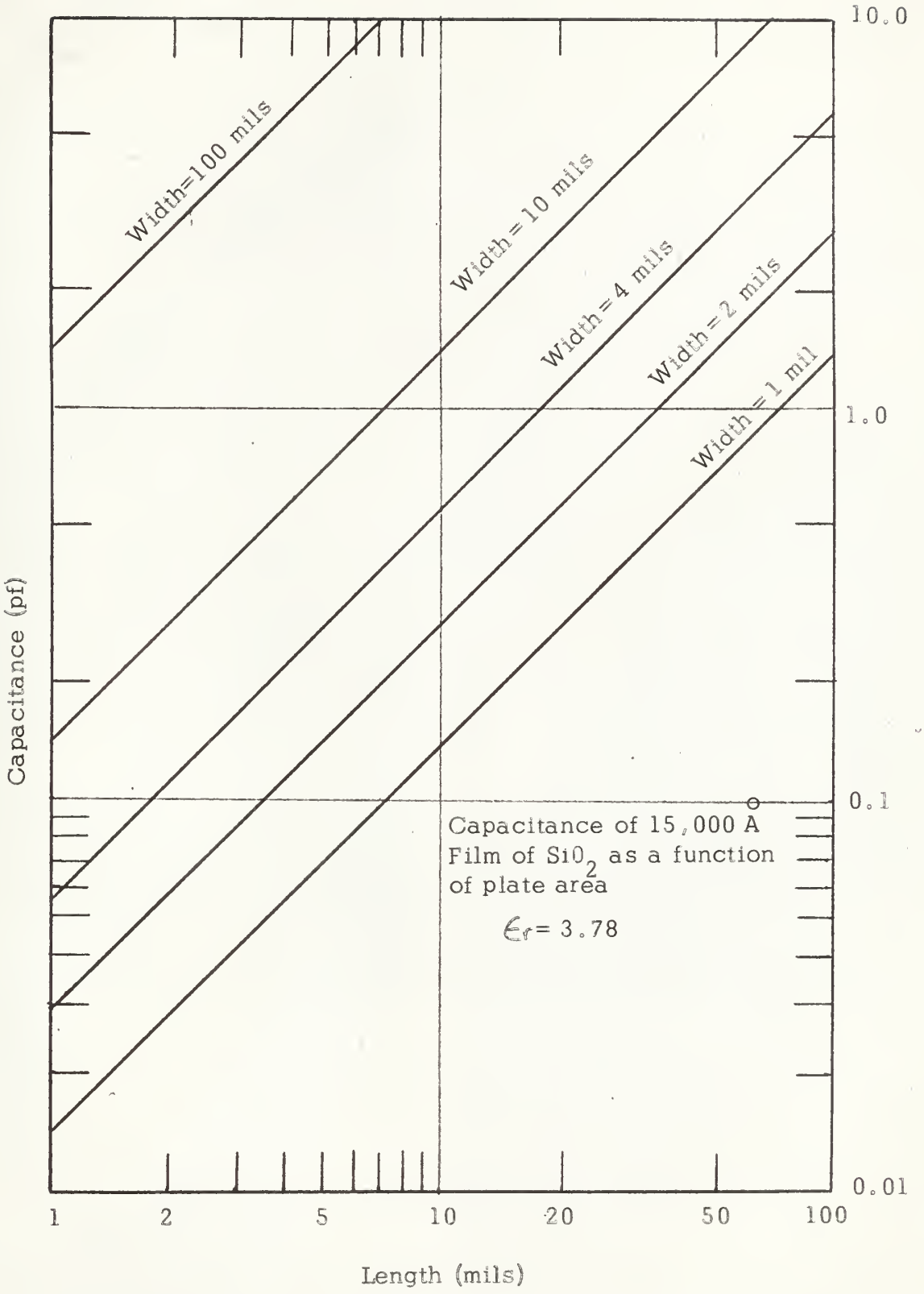


Fig. 13 Graph of Total Distributed Capacitance vs Length for Thin-Film Resistors

Fig. 14 Graph of Current Gain vs Frequency (Grounded Substrate)

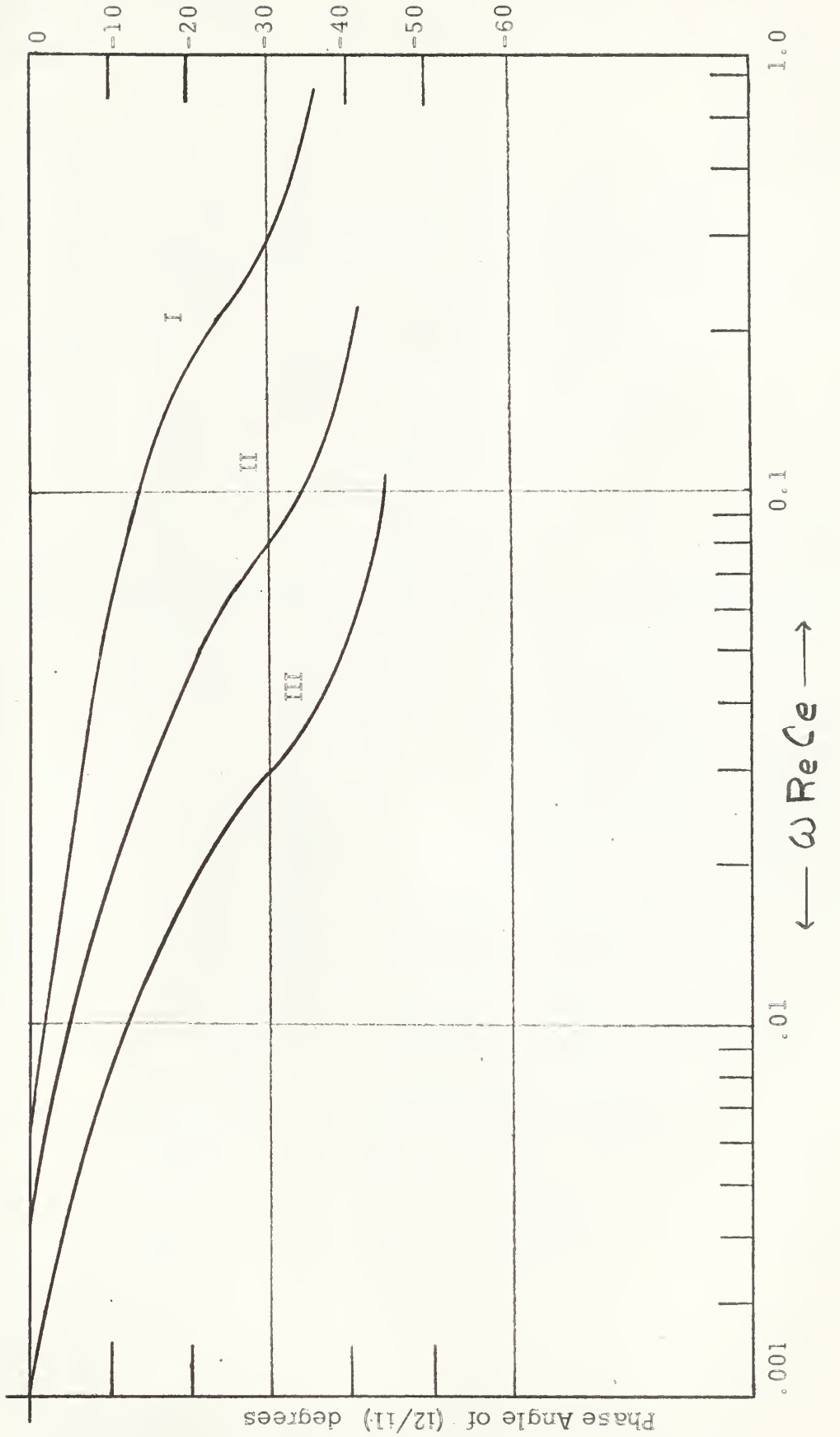


Fig. 15 Graph of Phase Angle vs Frequency (Grounded Substrate)

Fig. 16 Graph of Current Gain vs Frequency (Isolated Substrate)

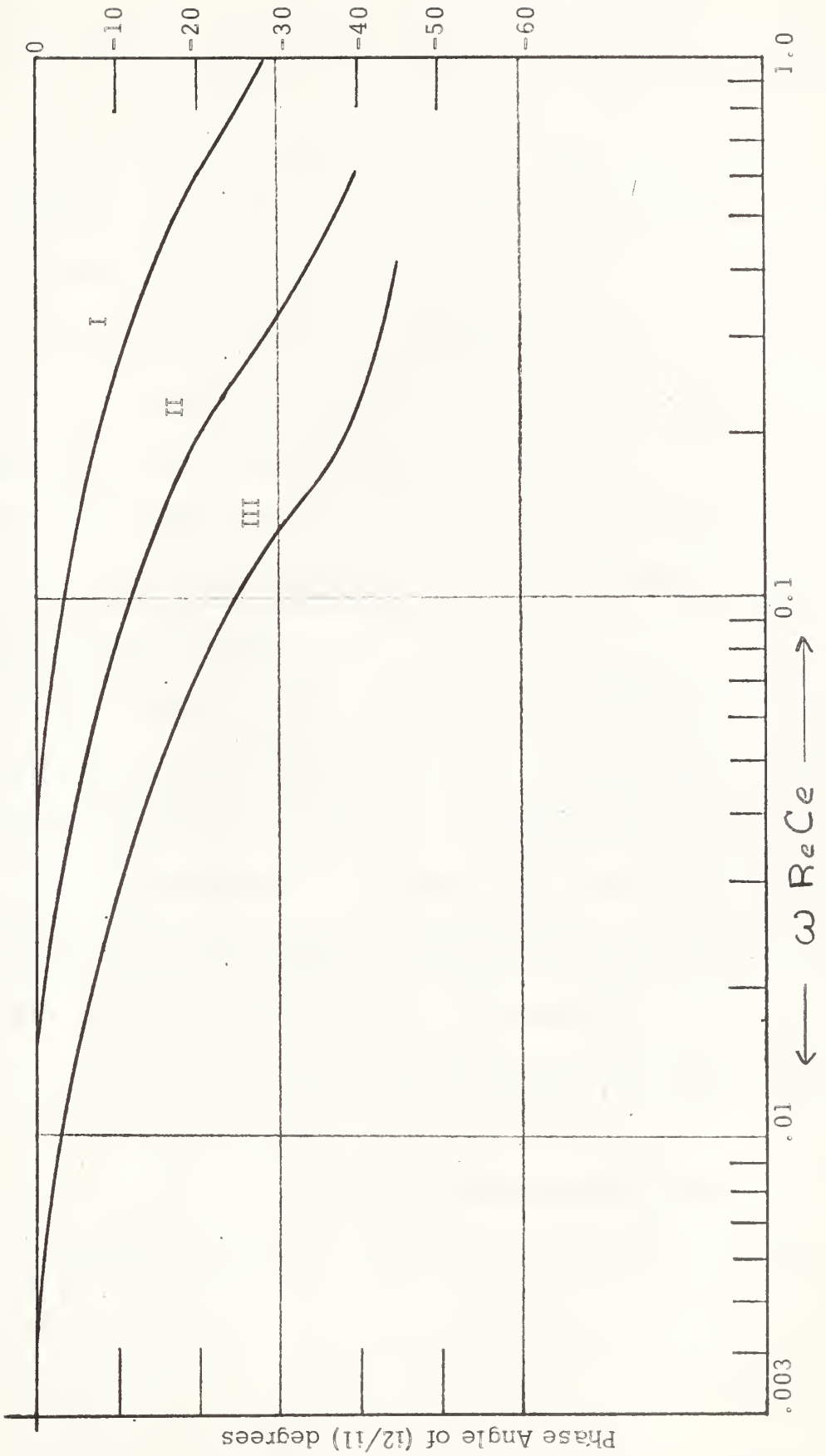


Fig. 17 Graph of Phase Angle vs Frequency (Isolated Substrate)

6. CONCLUSIONS AND COMMENTS

In order to fully exploit the potentialities of microelectronics for both digital and analog applications, old philosophies, old concepts and circuitry figures of merit must be reexamined and possibly revised to fit the needs of this rapidly expanding technology. The foregoing studies are indicative of the types of investigation which must be conducted to gain a more complete understanding of the assets and limitations associated with linear microcircuitry.

It has been shown how the "old" transmission line theory may be used to define the impedance functions for the distributed parameter thin-film resistive elements.

By way of a sample calculation the problem of finding how much junction capacitance is introduced, when producing integrated transistors with diffused junctions, was treated. It was shown that this output capacitance may be reduced by a judicial choice of biasing potentials. Also tucked away in the calculations, one can see that the geometry of the transistor plays an important role in determining the capacitance values. Further investigation into this aspect may prove most rewarding to the circuit design engineer.

The small signal analysis of a very simple amplifier stage points out the mathematical complexity of even the simplest of circuits when dealing with microcircuit concepts. Analytical models especially adapted to microcircuits are needed. The "old" theory of transistor

circuits should prove suitable for the very simple circuits, but the complexity associated with the inclusion of intercoupling effects and other interactions make it advisable to find new models for defining microelectronic parameters. A major study directed toward this good is currently underway at the Battelle Memorial Institute in Columbus, Ohio /3/.

In the circuit analysis presented, the assumption was made that sufficient reverse bias was applied to the collector-substrate junctions to keep the associated capacitance small enough to be neglected. Recent literature indicates that a new process is soon to be available whereby the junction isolation problem may be eliminated by using an extremely low capacitance per unit area dielectric with a very high breakdown voltage for isolation regions /15/.

Because of the limited time and funds for the research for this report, experimental microcircuitry was not made available for the results of the mathematical analysis to be experimentally verified or compared.

The following suggestions are offered to assist in furthering the investigations of the type begun herein:

(a) Attempt to mathematically show the effects of cascading two or more microcircuit amplifier stages.

(b) Find the effects of various biasing arrangements on the circuit response. It appears that thin-film elements employed in biasing net-

works will have some effect on frequency-sensitive circuits.

(c) Until such time as the production techniques designed to eliminate isolation junction capacitance are perfected, analysis of circuits which are to be powered by low-voltage sources (low reverse bias available) will require inclusion of the effects of this capacitance.

Microelectronics has developed from evolutionary rather than revolutionary ideas. It is therefore expected that the first steps in defining sophisticated microcircuit analytical models will be developed from existing circuit theory.

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APPENDIX A

Development of Magnitude and Phase Angle Equations for Distributed R-C Network Impedances /20/.

Case I, Grounded Substrate:

Given: $$\mathcal{Z} = \frac{R}{\theta} \tanh \theta$$

where $$\theta = (j\omega RC)^{1/2} \quad \text{and} \quad (j)^{1/2} = \frac{1+j}{\sqrt{2}}$$

Let $$q = \sqrt{\frac{\omega RC}{2}}$$

Then

$$\mathcal{Z} = \frac{R}{q(1+j)} \tanh (q + jq)$$

$$= \frac{R}{q+jq} \left[\frac{\sinh 2q + j \sin 2q}{\cosh 2q + \cos 2q} \right]$$

$$|\mathcal{Z}| = \frac{R}{q\sqrt{2}} \left[\frac{\sinh^2 2q - \sin^2 2q}{(\cosh 2q + \cos 2q)^2} \right]^{1/2}$$

$$= \frac{R}{q\sqrt{2}} \left[\frac{\cosh^2 2q - \cos^2 2q}{(\cosh 2q + \cos 2q)^2} \right]^{1/2}$$

$$= \frac{R}{q\sqrt{2}} \left[\frac{\cosh 2q - \cos 2q}{\cosh 2q + \cos 2q} \right]^{1/2}$$

but, $$q = \sqrt{\frac{\omega RC}{2}}$$

Therefore,

$$|Z| = \frac{R}{\sqrt{\omega RC}} \left[\frac{\cosh\sqrt{2\omega RC} - \cos\sqrt{2\omega RC}}{\cosh\sqrt{2\omega RC} + \cos\sqrt{2\omega RC}} \right]^{1/2}$$

$$\phi(Z) = \tan^{-1} \frac{Im[Z]}{Re[Z]}$$

$$Z = \frac{R}{q+jq} \left[\frac{\sinh 2q + j \sin 2q}{\cosh 2q + \cos 2q} \right]$$

$$= \frac{R}{q+jq} \left(\frac{\sinh 2q + j \sin 2q}{\cosh 2q + \cos 2q} \right) \left(\frac{q-jq}{q-jq} \right)$$

$$= \frac{R}{2q^2} \left[\frac{q \sinh 2q + jq \sin 2q - jq \sinh 2q + q \sin 2q}{\cosh 2q + \cos 2q} \right]$$

$$= \frac{R}{2q} \left[\frac{\sinh 2q + \sin 2q + j \sin 2q - \sinh 2q}{\cosh 2q + \cos 2q} \right]$$

$$= Re[Z] + j\, Im[Z]$$

Whence,

$$\measuredangle(Z) = \left[\frac{\sin 2\beta - \sinh 2\beta}{\sin 2\beta + \sinh 2\beta}\right]$$

Again,

$$\beta = \sqrt{\frac{\omega RC}{2}}$$

so

$$\measuredangle(Z) = \tan^{-1}\left[\frac{\sin\sqrt{2\omega RC} - \sinh\sqrt{2\omega RC}}{\sin\sqrt{2\omega RC} + \sinh\sqrt{2\omega RC}}\right]$$

Case II, Isolated Substrate:

Given:

$$Z = \frac{2R}{\theta}\tanh\frac{\theta}{2}$$

where

$$\theta = (j\omega RC)^{1/2} \quad \text{and} \quad (j)^{1/2} = \frac{1+j}{\sqrt{2}}$$

Here, let

$$\beta' = \sqrt{\frac{\omega RC}{2}}$$

then,

$$Z = \frac{2R}{\beta'(1+j)}\left[\tanh\left(\frac{\beta'}{2} + j\frac{\beta'}{2}\right)\right]$$

$$Z = \frac{2R}{q'+jq'}\left[\frac{\sinh q' + j\sin q'}{\cosh q' + \cos q'}\right]$$

$$|Z| = \frac{2R}{\sqrt{2}\,q'}\left[\frac{\sinh^2 q' - \sin^2 q'}{(\cosh q' + \cos q')^2}\right]^{1/2}$$

$$= \frac{2R}{\sqrt{2}\,q'}\left[\frac{\cosh^2 q' - \cos^2 q'}{(\cosh q' + \cos q')^2}\right]^{1/2}$$

$$= \frac{2R}{\sqrt{2}\,q'}\left[\frac{\cosh q' - \cos q'}{\cosh q' + \cos q'}\right]^{1/2}$$

but, $$q' = \sqrt{\frac{\omega RC}{2}}$$

thus,

$$|Z| = \frac{2R}{\sqrt{\omega RC}}\left[\frac{\cosh\sqrt{\frac{\omega RC}{2}} - \cos\sqrt{\frac{\omega RC}{2}}}{\cosh\sqrt{\frac{\omega RC}{2}} + \cos\sqrt{\frac{\omega RC}{2}}}\right]^{1/2}$$

As before, phase angle may be found from the relationship

$$\phi(Z) = \tan^{-1}\frac{Im[Z]}{Re[Z]}$$

so,

$$\phi(Z) = \tan^{-1}\left[\frac{\sin\sqrt{\frac{\omega RC}{2}} - \sinh\sqrt{\frac{\omega RC}{2}}}{\sin\sqrt{\frac{\omega RC}{2}} + \sinh\sqrt{\frac{\omega RC}{2}}}\right]$$

APPENDIX B

The fabrication of microcircuits is a lengthy process. The circuit designer cannot pick components "off the shelf" to construct circuits as was done with discrete component circuitry. A number of procedural steps are taken from the time a circuit is mentally conceived until the pilot model is ready for testing.

This author, during his visit with the Semiconductor Division of Hughes Aircraft Company, observed the operations and discussed, with technical personnel and engineers, the techniques involved in making hybrid integrated microcircuitry. The following compilation of procedural steps stems from these observations and discussions.

Procedural Steps for Fabrication of Hybrid-Integrated Microcuits

1. Design the circuit, observing microcircuit limitations.
2. Prepare art work for component and wiring topological layout.
3. Prepare circuit patterns into multi-layered mask pattersn from which glass or metal masks are to be made.
4. By photoreduction process, make the required masks.
5. Obtain P-type silicon wafers, sliced, lapped and etched smooth, and, in this case, with an epitaxially grown layer of N-type silicon over the P-type wafer.
6. Oxidize wafers in a high temperature, wet-oxygen atmosphere.
7. Photoengrave oxide with "fence" or isolation pattern.
8. Deposit and diffuse boron (P doping) in isolation pattern.

9. Photoengrave oxide with transistor base mask.
10. Deposit and diffuse boron (P-doping) for desired base depth.
11. Photoengrave oxide with emitter mask.
12. Deposit and diffuse phosphorus (N-doping) to desired emitter depth.
13. Etch oxide from back side of wafer.
14. Evaporate gold on back of wafer.
15. Diffuse gold throughout wafer, then lap excess gold from back of wafer.
16. Mask wafer for oxide removal to expose areas for interconnection contacts.
17. Evaporate aluminum over entire surface.
18. Photoengrave interconnection pattern.
19. Alloy aluminum for good adhesion and ohmic contacts.
20. Etch wafer with KOH to remove aluminum oxide.
21. Evaporate resistor material to wafer using resistor mask.
22. Scribe and break wafer into dice.
23. Sort dice for packaging.
24. Attach die to package header.
25. Bond leads (gold or aluminum wire) to die and weld to package leads.
26. Clean and seal.
27. Test completed item.

For the sake of brevity, several intermediate cleaning and testing

steps were omitted here. It should be obvious that with the number of possible steps where failure of the element might occur, constant testing is a necessity. All efforts are made to keep the units clean throughout processing. Special clean rooms (white rooms) are maintained where all microcircuit procedures are carried on.

Normal processing through the steps outlined may take from two to three weeks.

Fig. 18 shows a circuit produced in the manner just described. The silicon integrated circuit pictured is interconnected to form a TTL gate. The circuit, produced by the Semiconductor Division of Hughes Aircraft Company is called a "Quadralogic" circuit. Each quadrant of the circuit contains one four emitter and three single emitter NPN transistors with 4 thin-film nichrome resistors. Each quadrant is capable of being connected as a complete 4 input NAND or NOR logic gate. Variation in circuit functions may be obtained by changing interconnection or resistor masks in the fabrication process.

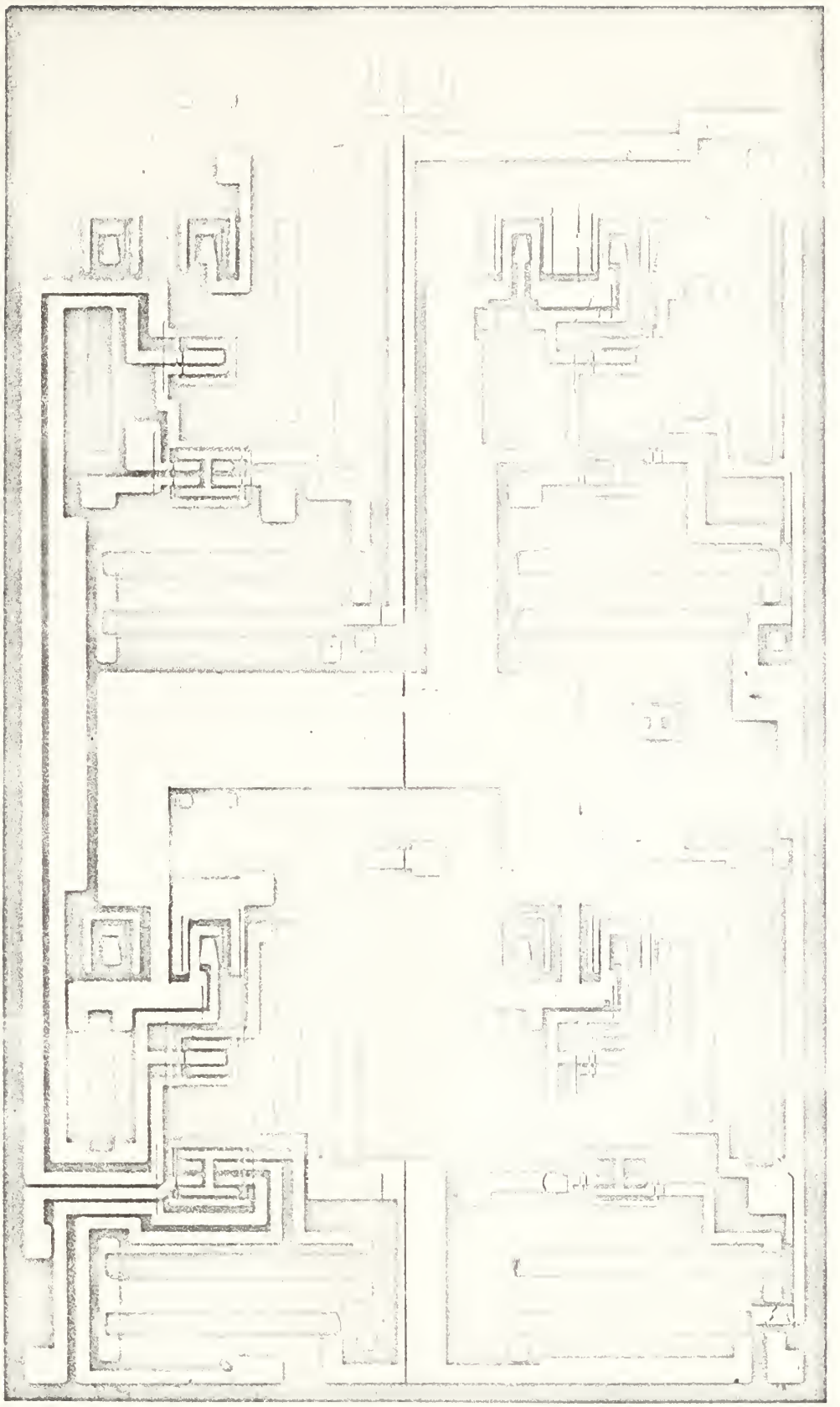

Fig. 18 A Hybrid Integrated Microcircuit--"Quadralogic" Circuit of Hughes Aircraft Company
(courtesy Semiconductor Division, Hughes Aircraft Company)